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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,366	SERA, HIROSHI	
	Examiner	Art Unit	
	Colleen E. Rodgers	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Amendment filed 26 November 2007. By this amendment, claims 13-18 are added. No claims are amended or canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6, 8-15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al** (US Patent Application Publication 2002/0145142) in view of **Suzuki** (USPN 7,087,963).

Regarding claims 1, 10 and 13, **Chen et al** teach a method of forming a thin-film semiconductor device including a semiconductor film having a source region, a channel region and a drain region, a gate electrode opposing the semiconductor film and a gate-insulating film disposed between the semiconductor film and the gate electrode, the source region and the drain region further including a region with a relatively high impurity concentration and a region with a relatively low impurity concentration, respectively, the method including the steps of:

forming a semiconductor film **32** with a predetermined pattern on a substrate **30**;

forming a gate-insulating film **34** on the semiconductor film **32**;

forming a tapered gate electrode **36** on the gate insulating film **34** [see paragraph 0019, wherein it is noted that the gate electrode may be trapezoidal rather than rectangular];

implanting a low concentration of impurity into the semiconductor film **32** through the gate electrode **36** functioning as a mask [see paragraph 0020];

forming a layered insulating film composed of at least two different insulating films **40**, **42** on the gate electrode **36** on the substrate **30**, the second insulating film **42** having a different composition from the first insulating film **40**;

etching an entire surface of the layered insulating film to form a predetermined pattern in at least one of the layers **42** of the layered insulating film, the predetermined pattern having a width greater than a width of the gate electrode **36** and smaller than a width of the substrate **30** [see Fig. 2D]; and

implanting a high concentration of impurity through the layered insulating film formed according to a predetermined pattern functioning as a mask [see paragraph 0021].

Chen et al do not disclose that the gate electrode is tapered at a 20° to 80° angle. These claims are *prima facie* obvious without a showing that the claimed angles achieve unexpected results relative to the prior art angles. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art in general conditions is obvious). In this case, there exists no evidence of record that the angle of tapering provides unexpected results in the gate electrode produced. One of ordinary skill in the art would be motivated to optimize the taper angle to provide for device performance.

Furthermore, **Chen et al** do not teach the composition of the gate insulating film, and therefore do not disclose wherein the first insulating film is formed of a different composition than the gate insulating film. **Suzuki** teaches a substantially similar method, including forming a semiconductor film **12** with a predetermined pattern on a substrate **10**, forming a gate-insulating film **13** on the semiconductor film, the gate insulating film being composed of silicon oxide [see col. 1, lines 52-55], forming a gate electrode **15** on the gate-insulating film, forming a layered insulating film composed of at least two different insulating layers **19**, **20** on the gate electrode on the substrate, the first insulating layer **19** (silicon nitride) having different composition from the gate-insulating film and the second insulating layer **20** (silicon oxide) having different composition from the first insulating layer [see col. 2, lines 14-18]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the materials taught by **Suzuki** in the method taught by **Chen et al** because these materials are well known in the art for these purposes and furthermore because this configuration beneficially provides etch selectivity when the materials are provided as taught by **Suzuki** in the order oxide-nitride-oxide.

Finally, neither **Chen et al** nor **Suzuki** disclose specifically wherein the second insulating film has a thickness of more than twice the thickness of the gate electrode (although Fig. 3 of **Suzuki** would seem to indicate as such, it is not necessarily assumed that these drawings are to scale). However, these claims are *prima facie* obvious without a showing that the claimed ranges achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of

result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art in general conditions is obvious). In this case, there exists no evidence of record that the relative thicknesses provide unexpected results in the semiconductor device produced. One of ordinary skill in the art would be motivated to optimize the relative thicknesses to provide for processing limitations and device performance.

Regarding claims 2 and 14, the prior art of **Chen et al** and **Suzuki** disclose the methods of claims 1 and 13 as described above. Furthermore, **Chen et al** disclose wherein the uppermost layer **42** of the layered insulating film is isotropically formed and anisotropically etched [see Figs. 2C and 2D].

Regarding claim 3, the prior art of **Chen et al** and **Suzuki** disclose the method of claim 1 as described above. Furthermore, **Chen et al** disclose wherein anisotropic etching is performed after the formation of the predetermined pattern as shown in Fig. 2D, the predetermined pattern having a width greater than the width of the gate electrode **36** and smaller than the width of the semiconductor film **32** [see Fig. 2E].

Regarding claim 4, **Chen et al** teach a method of forming a thin-film semiconductor device including a semiconductor film having a source region, a channel region and a drain region, a gate electrode opposing the semiconductor film and a gate-insulating film disposed between the semiconductor film and the gate electrode, the source region and the drain region further including a region with a relatively high impurity concentration and a region with a relatively low impurity concentration, respectively, the method including the steps of:

forming a semiconductor film **32** with a predetermined pattern on a substrate **30**;

forming a gate-insulating film **34** on the semiconductor film **32**;

forming a tapered gate electrode **36** on the gate insulating film **34** [see paragraph 0019, wherein it is noted that the gate electrode may be trapezoidal rather than rectangular];

implanting a low concentration of impurity into the semiconductor film **32** through the gate electrode **36** functioning as a mask [see paragraph 0020];

forming a layered insulating film composed of at least two different insulating films **40, 42** on the gate electrode **36** on the substrate **30**, the second insulating film **42** having a different composition from the first insulating film **40**;

etching an entire surface of the layered insulating film to form a predetermined pattern in at least one of the layers **42** of the layered insulating film, the predetermined pattern having a width greater than a width of the gate electrode **36** and smaller than a width of the substrate **30** [see Fig. 2D];

forming a sidewall against the tapered gate electrode, the sidewall composed of two different layers of the layered insulating film [see Figs. 2E and 2F]; and

implanting a high concentration of impurity through the layered insulating film formed according to a predetermined pattern functioning as a mask [see paragraph 0021].

Chen et al do not teach the composition of the gate insulating film, and therefore do not disclose wherein the first insulating film is formed of a different composition than the gate insulating film, nor wherein the second insulating layer and the gate-insulating layer have substantially the same composition. **Suzuki** teaches a substantially similar method, including forming a semiconductor film **12** with a predetermined pattern on a substrate **10**, forming a gate-insulating film **13** on the semiconductor film, the gate insulating film being composed of silicon oxide [see col. 1, lines 52-55], forming a gate electrode **15** on the gate-insulating film, forming a layered insulating film composed of at least two different insulating layers **19, 20** on the gate electrode on the substrate, the first

insulating layer **19** (silicon nitride) having different composition from the gate-insulating film and the second insulating layer **20** (silicon oxide) having different composition from the first insulating layer [see col. 2, lines 14-18]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the materials taught by **Suzuki** in the method taught by **Chen et al** because these materials are well known in the art for these purposes and furthermore because this configuration beneficially provides etch selectivity when the materials are provided as taught by **Suzuki** in the order oxide-nitride-oxide.

Furthermore, neither **Chen et al** nor **Suzuki** disclose specifically wherein the second insulating film has a thickness of more than twice the thickness of the gate electrode (although Fig. 3 of **Suzuki** would seem to indicate as such, it is not necessarily assumed that these drawings are to scale). However, these claims are *prima facie* obvious without a showing that the claimed ranges achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art in general conditions is obvious). In this case, there exists no evidence of record that the relative thicknesses provide unexpected results in the semiconductor device produced. One of ordinary skill in the art would be motivated to optimize the relative thicknesses to provide for processing limitations and device performance.

Regarding claims 6 and 17, the prior art of **Chen et al** and **Suzuki** disclose the methods of claims 1 and 13 as described above. Furthermore, **Chen et al** disclose wherein the etching rate of

the upper insulating layer is greater than the etching rate of the lower insulating layer in the first, dry-etching process (etch-selective to the uppermost insulating layer), and the etching rate of the exposed lower insulating layer is greater than the etching rate of the remaining upper insulating layer in the second, wet-etching process (etch-selective to the lower insulating layer). As best understood, it is inherent that in a process utilizing two etch steps, etch selectivity is practiced to control which material is etched by each process.

Regarding claims 8 and 18, the prior art of **Chen et al** and **Suzuki** disclose the methods of claims 1 and 13 as described above. Furthermore, **Suzuki** discloses wherein the layered insulating film further comprises a first insulating layer **19** composed of silicon nitride and a second insulating layer **20** composed of silicon oxide on the first insulating film [see col. 5, lines 28-33].

Regarding claims 9 and 11, the prior art of **Chen et al** and **Suzuki** disclose the method of claim 1 as described above. Furthermore, **Chen et al** disclose wherein the insulating film **40** is formed at least along the sides of the gate electrode **36** [see Figs. 2C-2F], and each of the source region and the drain region **48** of the semiconductor have a low-concentration region **38** corresponding to a portion of the insulating film **40** with a width grater than the width of the gate electrode **36** [see Fig. 2F].

Regarding claim 12, the prior art of **Chen et al** and **Suzuki** disclose the method of claim 1 as described above. Furthermore, Chen et al disclose wherein the resulting electro-optic apparatus may be included in an LCD display [see paragraph 0004].

Regarding claim 15, the prior art of **Chen et al** and **Suzuki** disclose the method of claim 13 as described above. **Chen et al** do not teach wherein the second insulating layer and the gate-insulating layer have substantially the same composition. **Suzuki** teaches a substantially similar method, including forming a semiconductor film **12** with a predetermined pattern on a substrate **10**,

forming a gate-insulating film **13** on the semiconductor film, the gate insulating film being composed of silicon oxide [see col. 1, lines 52-55], forming a gate electrode **15** on the gate-insulating film, forming a layered insulating film composed of at least two different insulating layers **19**, **20** on the gate electrode on the substrate, the first insulating layer **19** (silicon nitride) having different composition from the gate-insulating film and the second insulating layer **20** (silicon oxide) having different composition from the first insulating layer [see col. 2, lines 14-18]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the materials taught by **Suzuki** in the method taught by **Chen et al** because these materials are well known in the art for these purposes and furthermore because this configuration beneficially provides etch selectivity when the materials are provided as taught by **Suzuki** in the order oxide-nitride-oxide.

4. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al** (US Patent Application Publication 2002/0145142) in view of **Suzuki** (USPN 7,087,963) as applied to claims 1-4, 6, 8-15, 17 and 18 above, and further in view of **Guldi** (USPN 5,576,230).

Regarding claim 5, **Chen et al** teach a method of forming a thin-film semiconductor device including a semiconductor film having a source region, a channel region and a drain region, a gate electrode opposing the semiconductor film and a gate-insulating film disposed between the semiconductor film and the gate electrode, the source region and the drain region further including a region with a relatively high impurity concentration and a region with a relatively low impurity concentration, respectively, the method including the steps of:

forming a semiconductor film **32** with a predetermined pattern on a substrate **30**;

forming a gate-insulating film **34** on the semiconductor film **32**;

forming a tapered gate electrode **36** on the gate insulating film **34** [see paragraph 0019, wherein it is noted that the gate electrode may be trapezoidal rather than rectangular];

implanting a low concentration of impurity into the semiconductor film **32** through the gate electrode **36** functioning as a mask [see paragraph 0020];

forming a layered insulating film composed of at least two different insulating films **40, 42** on the gate electrode **36** on the substrate **30**, the second insulating film **42** having a different composition from the first insulating film **40**;

etching an entire surface of the layered insulating film to form a predetermined pattern in at least one of the layers **42** of the layered insulating film, the predetermined pattern having a width greater than a width of the gate electrode **36** and smaller than a width of the substrate **30** [see Fig. 2D];

implanting a high concentration of impurity through the layered insulating film formed according to a predetermined pattern functioning as a mask [see paragraph 0021].

Chen et al do not teach the composition of the gate insulating film, and therefore do not disclose wherein the first insulating film is formed of a different composition than the gate insulating film, nor wherein the second insulating layer and the gate-insulating layer have substantially the same composition. **Suzuki** teaches a substantially similar method, including forming a semiconductor film **12** with a predetermined pattern on a substrate **10**, forming a gate-insulating film **13** on the semiconductor film, the gate insulating film being composed of silicon oxide [see col. 1, lines 52-55], forming a gate electrode **15** on the gate-insulating film, forming a layered insulating film composed of at least two different insulating layers **19, 20** on the gate electrode on the substrate, the first insulating layer **19** (silicon nitride) having different composition from the gate-insulating film and the second insulating layer **20** (silicon oxide) having different composition from the first insulating layer

[see col. 2, lines 14-18]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the materials taught by **Suzuki** in the method taught by **Chen et al** because these materials are well known in the art for these purposes and furthermore because this configuration beneficially provides etch selectivity when the materials are provided as taught by **Suzuki** in the order oxide-nitride-oxide.

Furthermore, neither **Chen et al** nor **Suzuki** disclose specifically wherein the second insulating film has a thickness of more than twice the thickness of the gate electrode (although Fig. 3 of **Suzuki** would seem to indicate as such, it is not necessarily assumed that these drawings are to scale). However, these claims are *prima facie* obvious without a showing that the claimed ranges achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art in general conditions is obvious). In this case, there exists no evidence of record that the relative thicknesses provide unexpected results in the semiconductor device produced. One of ordinary skill in the art would be motivated to optimize the relative thicknesses to provide for processing limitations and device performance.

Finally, neither **Chen et al** nor **Suzuki** disclose that the etching is controlled via endpoint detection. However, **Guldi** teaches that endpoint detection is utilized in wet etching processes [see col. 5, lines 1-6]. It would have been obvious to one of ordinary skill in the art at the time of

invention to employ an endpoint detection process as taught by **Guldi** in the method of **Chen et al** and **Suzuki** to prevent either under- or over-etching of the insulating film.

Regarding claim 16, the prior art of **Chen et al** and **Suzuki** disclose the method of claim 13 as described above. Neither **Chen et al** nor **Suzuki** disclose that the etching is controlled via endpoint detection. However, **Guldi** teaches that endpoint detection is utilized in wet etching processes [see col. 5, lines 1-6]. It would have been obvious to one of ordinary skill in the art at the time of invention to employ an endpoint detection process as taught by **Guldi** in the method of **Chen et al** and **Suzuki** to prevent either under- or over-etching of the insulating film.

Response to Arguments

5. Applicant's arguments filed 26 November 2007 have been fully considered but they are not persuasive. On page 10 of the Remarks, Applicant alleges that "… Applicant has adequately disclosed unanticipated benefits of the claimed features," but the Examiner disagrees. Applicant has merely asserted unanticipated benefits, which is not sufficient. As the Examiner has stated several times, Applicant has not provided any **evidence** that the claimed angle produces some unexpected result. Indeed, the claimed range of a tapering angle of 20° to 80° includes all but the extremes, and it seems clear that almost any tapered gate would meet this limitation.

On page 11 of the Remarks, Applicant goes on to state that "… Applicant stated that such relative thickness of the second insulating layer provides for a relatively long lightly doped drain (LDD), as described, for example, in … Applicant's specification." Again, Applicant has merely asserted unanticipated benefits, which is not sufficient. As the Examiner has stated several times, Applicant has not provided any **evidence** that the relative thicknesses achieve a length of LDD that is unachievable by the cited art. Furthermore, as noted by the Examiner, the cited art of **Suzuki**

appears to satisfy the claimed limitation in the depiction of Fig. 3. Finally, Applicant's assertion that the LDD formed thus is "relatively" long does not adequately describe the metes and bounds of the invention in any case.

On pages 12-13 of the Remarks, Applicant alleges that the cited art of **Suzuki** is deficient because of the inclusion of a further dielectric layer **14** formed beneath the gate **15**, and thus "no identified intended benefit of the specific compositions in Suzuki would have motivated one of ordinary skill in the art to modify the Chen method or apparatus in the manner suggested." The Examiner vehemently disagrees for a variety of reasons: first, the supposed deficiency of **Suzuki**, wherein the dielectric layer **14** is interposed between the gate dielectric **13** and the gate **15**, is immaterial because **Suzuki** has not been applied under 35 U.S.C. §102, but rather under 35 U.S.C. §103. **Suzuki** was combined with **Chen et al** to teach material choice, not configuration. Secondly, there is no impediment to putting a gate directly on a silicon dioxide gate-insulating layer, as is notoriously well-known in the art, and as the silicon nitride layer **14** is not exposed beneath the gate, the cited benefit (i.e., increased etching selectivity) still applies. Furthermore, choosing an oxide-nitride-oxide configuration for the claimed structure is not novel because it has been held that simple substitution of one known material for another to obtain predictable results is obvious. See *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the

mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen E. Rodgers whose telephone number is (571) 272-8603. The examiner can normally be reached on Monday through Friday, 8:00 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Carl Whitehead Jr./
Supervisory Patent Examiner, Art Unit 2813

/C. E. R./
Examiner, Art Unit 2813